**Memory and Peripherals Interfacing**

Abstract of this topic:

1.1 Memory Interfacing – RAM and ROM Decoding Techniques – Partial and Absolute: Memory interfacing is a key part of microprocessor design, as it allows the microprocessor to access additional memory beyond what is integrated on the chip. RAM (Random Access Memory) and ROM (Read-Only Memory) are two types of memory that can be interfaced with a microprocessor. RAM is volatile memory that can be read from and written to, while ROM is non-volatile memory that can only be read from.

Decoding techniques are used to identify the specific memory location being accessed by the microprocessor. Partial decoding involves selecting a portion of the address lines to decode, while absolute decoding involves decoding the entire address. The choice of decoding technique depends on the specific system design and requirements.

1.2 8255-PPI-Block diagram, CWR, Operations modes, interfacing with 8086: The 8255 is a Programmable Peripheral Interface (PPI) chip that can be used to interface various peripheral devices with the microprocessor. It provides three ports (A, B, and C), each with 8 input/output lines.

The Control Word Register (CWR) is used to configure the operation of the 8255, specifying the modes of operation and other parameters. There are three modes of operation: mode 0 (basic input/output), mode 1 (strobe input/output), and mode 2 (bidirectional bus). The 8255 can be interfaced with an 8086 microprocessor using the Address Bus, Data Bus, and Control Bus.

1.3 8257-DMAC Block diagram, DMA operations and transfer modes: The 8257 is a Direct Memory Access Controller (DMAC) chip that can be used to improve data transfer performance between memory and peripheral devices. It allows data transfer to occur directly between peripheral devices and memory, bypassing the microprocessor.

The 8257 has a block diagram that includes control and status registers, a mode set register, a request register, and a terminal count register. DMA (Direct Memory Access) operations involve the DMAC transferring data between the peripheral device and memory without the microprocessor's intervention. The transfer modes include single transfer, block transfer, demand transfer, and cyclic transfer.

1.4 Programmable Interrupt Controller 8259-Block Diagram, Interfacing the 8259 in single and cascaded mode: The 8259 is a Programmable Interrupt Controller (PIC) that is used to manage interrupts in the system. Interrupts are signals sent to the microprocessor by peripheral devices to request attention. The 8259 can prioritize and manage multiple interrupt requests, allowing the microprocessor to respond to them in the correct order.

The 8259 has a block diagram that includes interrupt request lines, interrupt service registers, interrupt mask registers, and an interrupt control register. The 8259 can be interfaced with the microprocessor in single mode or cascaded mode. In single mode, only one 8259 is used, while in cascaded mode, multiple 8259s are used together to handle a larger number of interrupt requests.

Overall, the topics covered in Module 3 of your microprocessor course provide a deeper understanding of memory and peripheral interfacing and their importance in microprocessor design. These concepts are critical for designing and developing efficient and effective microprocessor-based systems.